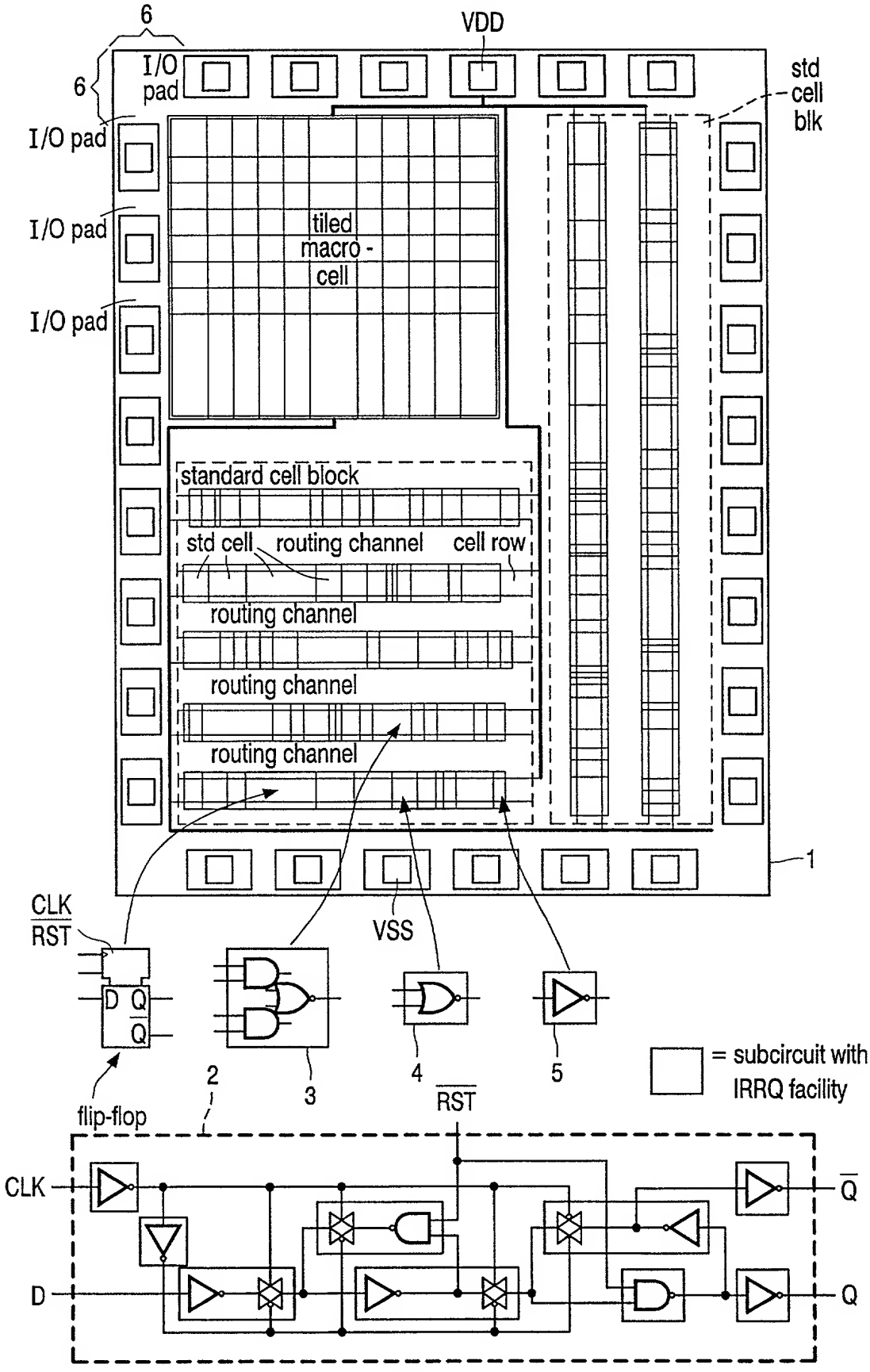
6
VDD
I/O pad
6
std cell blk
I/O pad
I/O pad
I/O pad
tiled macro - cell
standard cell block
std cell
routing channel
cell row
routing channel
routing channel
routing channel
1
CLK
RST
VSS
D
Q
Q
2
3
4
5
= subcircuit with IRRQ facility
flip-flop
RST
CLK
D
Q
Q

FIG. 1

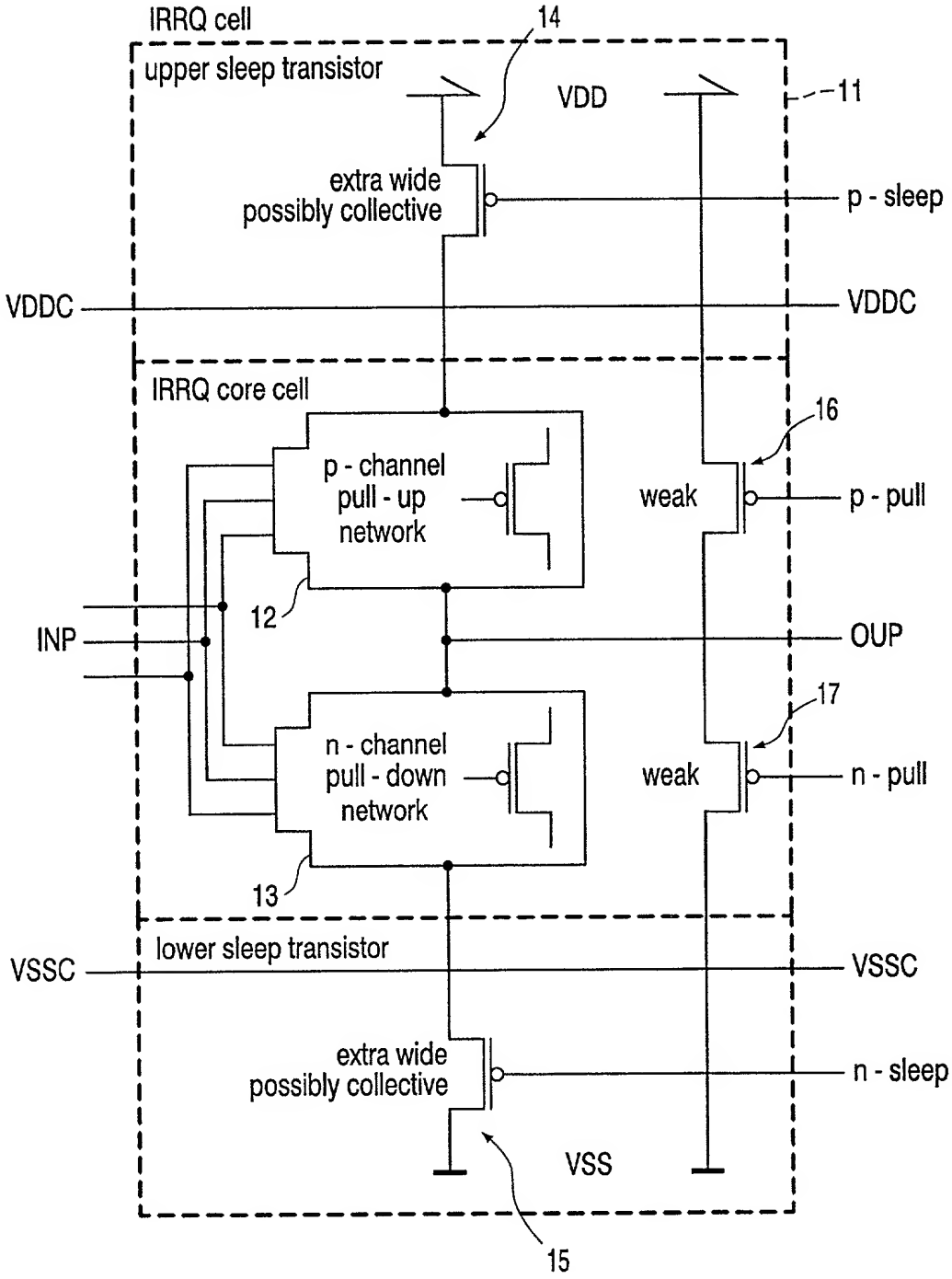
IRRQ cell
upper sleep transistor
14
VDD
11
extra wide
possibly collective
p - sleep
VDDC
VDDC
IRRQ core cell
16
p - channel
pull - up
network
weak
p - pull
12
INP
OUP
17
n - channel
pull - down
network
weak
n - pull
13
lower sleep transistor
VSSC
VSSC
extra wide
possibly collective
n - sleep
VSS
15

FIG. 2

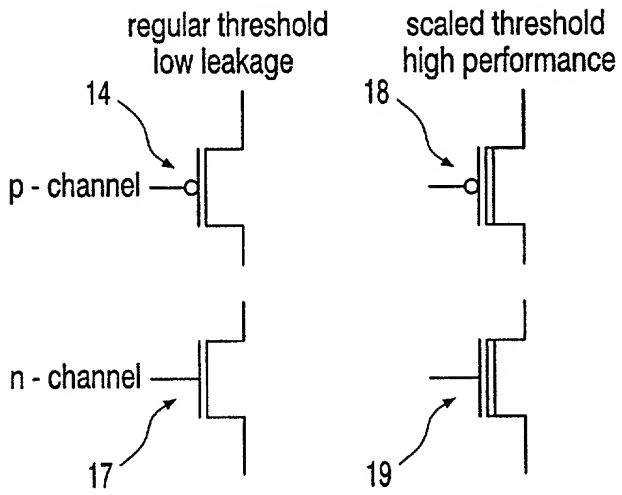
regular threshold
low leakage
scaled threshold
high performance
14
18
p - channel
n - channel
17
19

FIG. 3

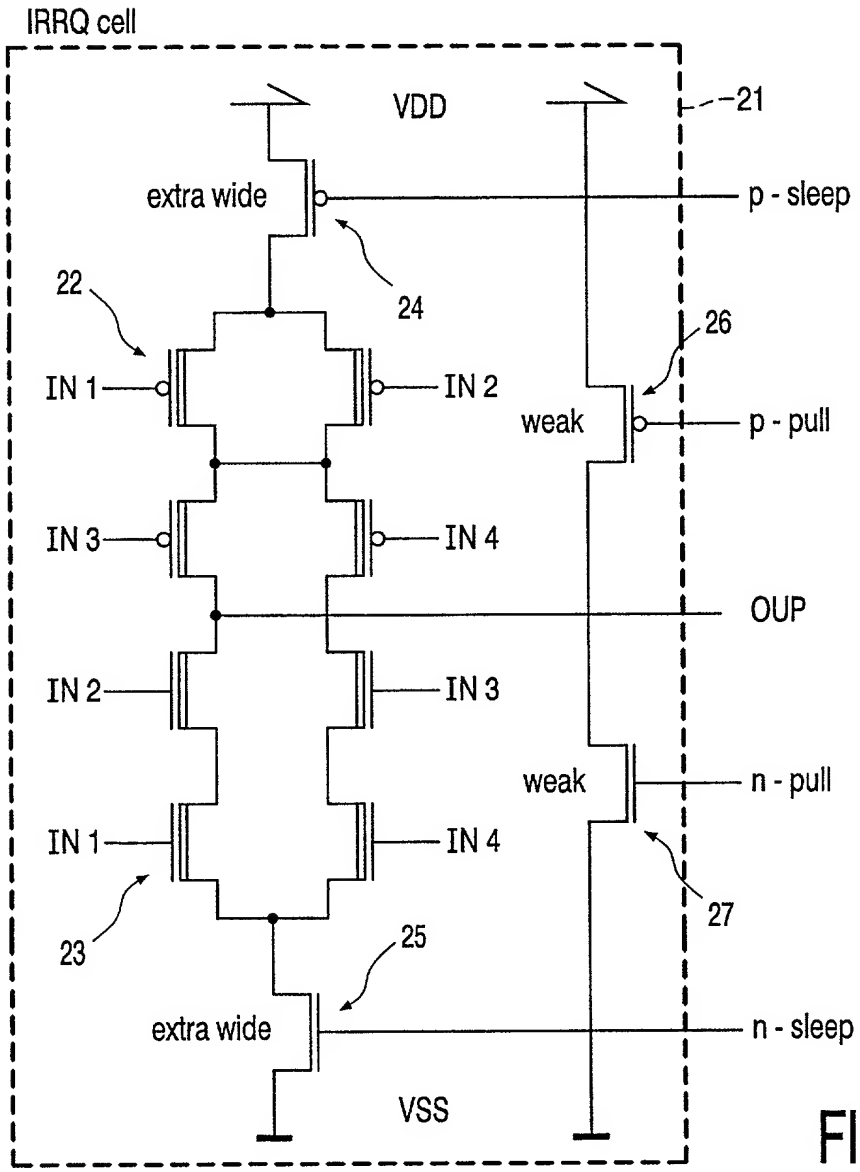
IRRQ cell
VDD
21
extra wide
p - sleep
22
24
26
IN 1
IN 2
weak
p - pull
IN 3
IN 4
OUP
IN 2
IN 3
weak
n - pull
IN 1
IN 4
23
25
27
extra wide
n - sleep
VSS

FIG. 4

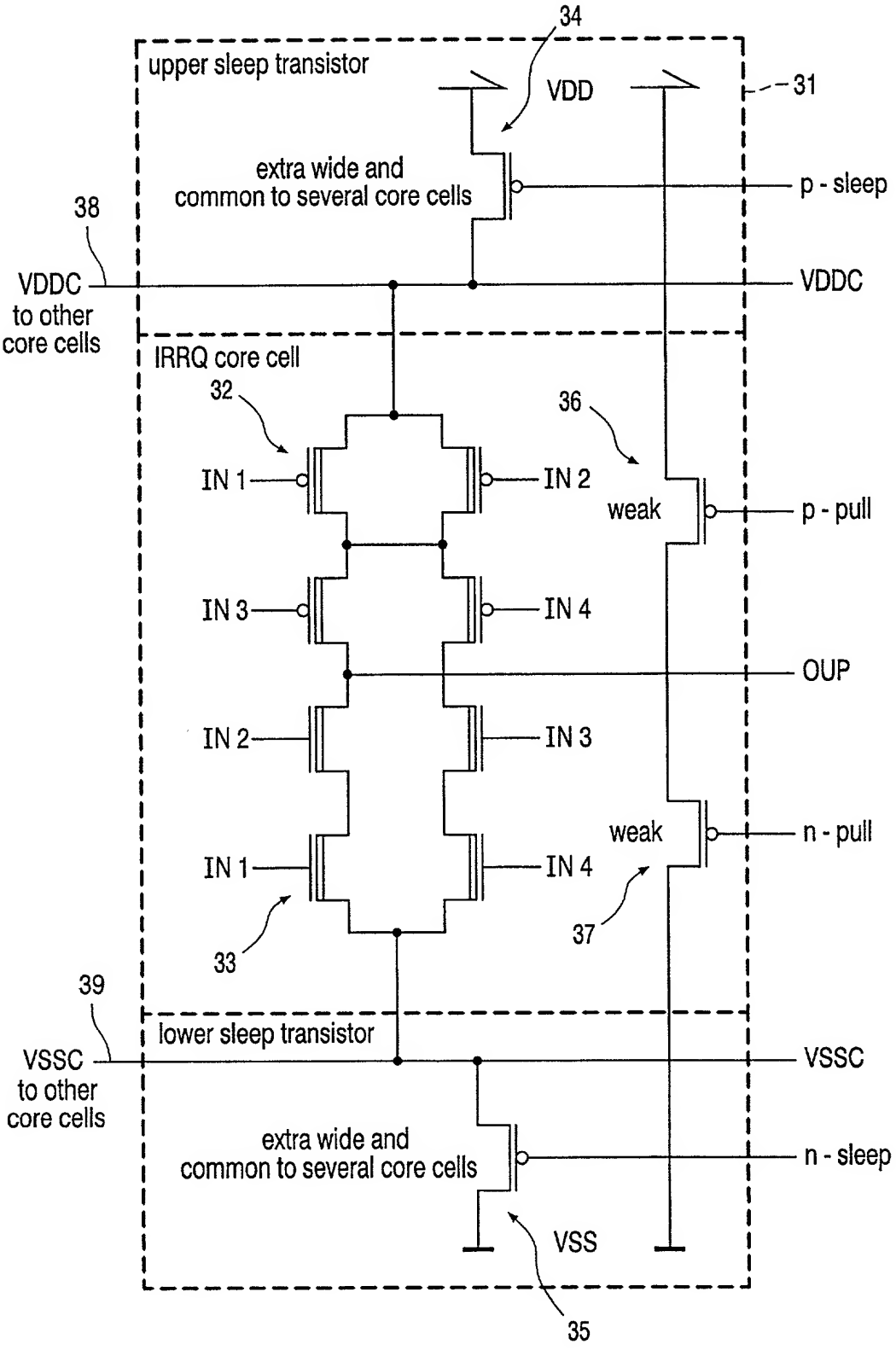
34
upper sleep transistor
VDD
31
extra wide and
common to several core cells
p - sleep
38
VDDC
to other
core cells
VDDC
IRRQ core cell
32
36
IN 1
IN 2
weak
p - pull
IN 3
IN 4
OUP
IN 2
IN 3
weak
n - pull
IN 1
IN 4
37
33
39
lower sleep transistor
VSSC
to other
core cells
VSSC
extra wide and
common to several core cells
n - sleep
VSS
35

FIG. 5

defect to be checked	n - netw.	p - netw.	n - sleep	n - pull	p - pull	p - sleep	I_{ddq}
within regular n - and p - channel networks							
n - channel open or short p - channel open or short	stimulate don't care	don't care stimulate	on off	off on	on off	off on	
within auxiliary transistors							
n - sleep open or short p - sleep open or short	on don't care	don't care on	toggle off	off on	on off	off toggle	
p - pull open p - pull short p - pull on (weak pull - up) or alternatively	on on on don't care	don't care don't care don't care don't care	toggle toggle on off	off off off on	on on off off	off off off off	 check idem
n - pull open n - pull short n - pull on (weak pull - dn) or alternatively	don't care don't care don't care don't care	on on on don't care	off off off off	on on off off	off off off on	toggle toggle on off	 check idem

FIG. 6

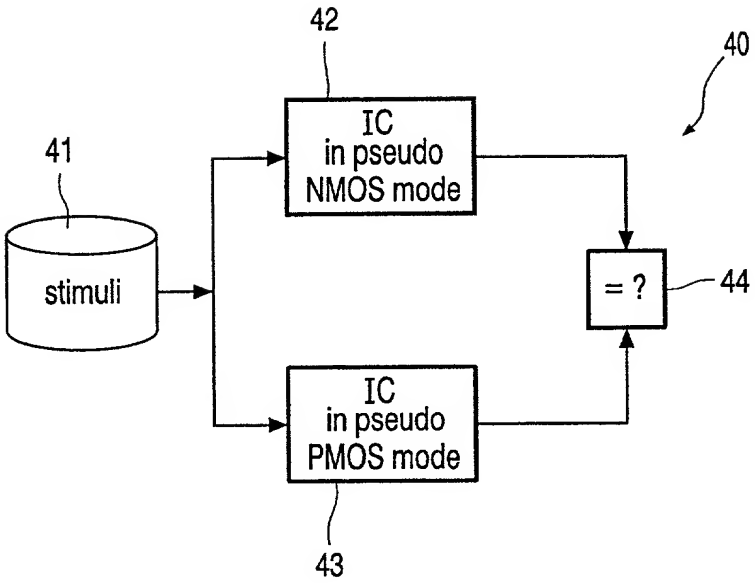
42
40
IC
in pseudo
NMOS mode
41
stimuli
= ?
44
IC
in pseudo
PMOS mode
43

FIG. 7A

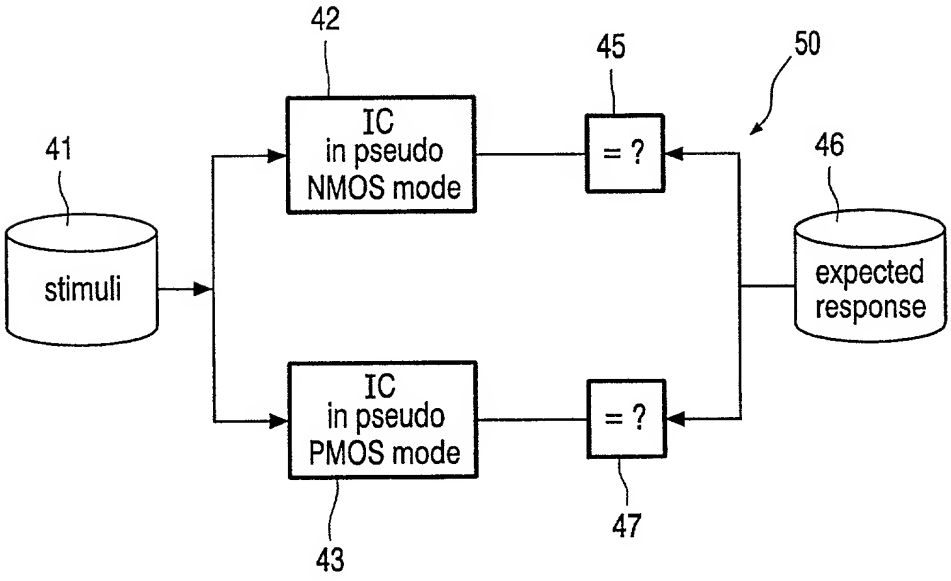
42
45
50
IC
in pseudo
NMOS mode
= ?
41
46
stimuli
expected
response
IC
in pseudo
PMOS mode
= ?
47
43

FIG. 7B